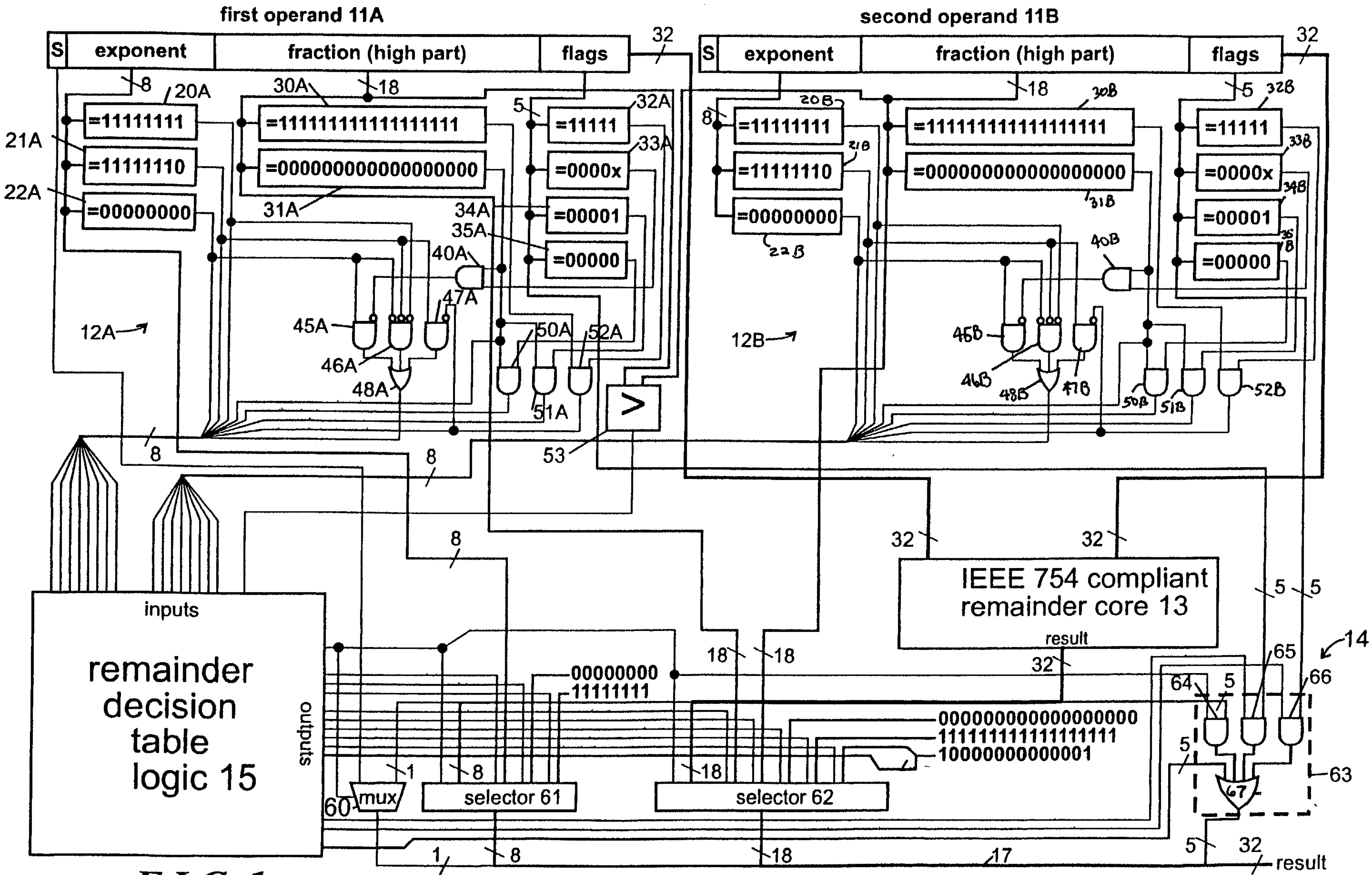
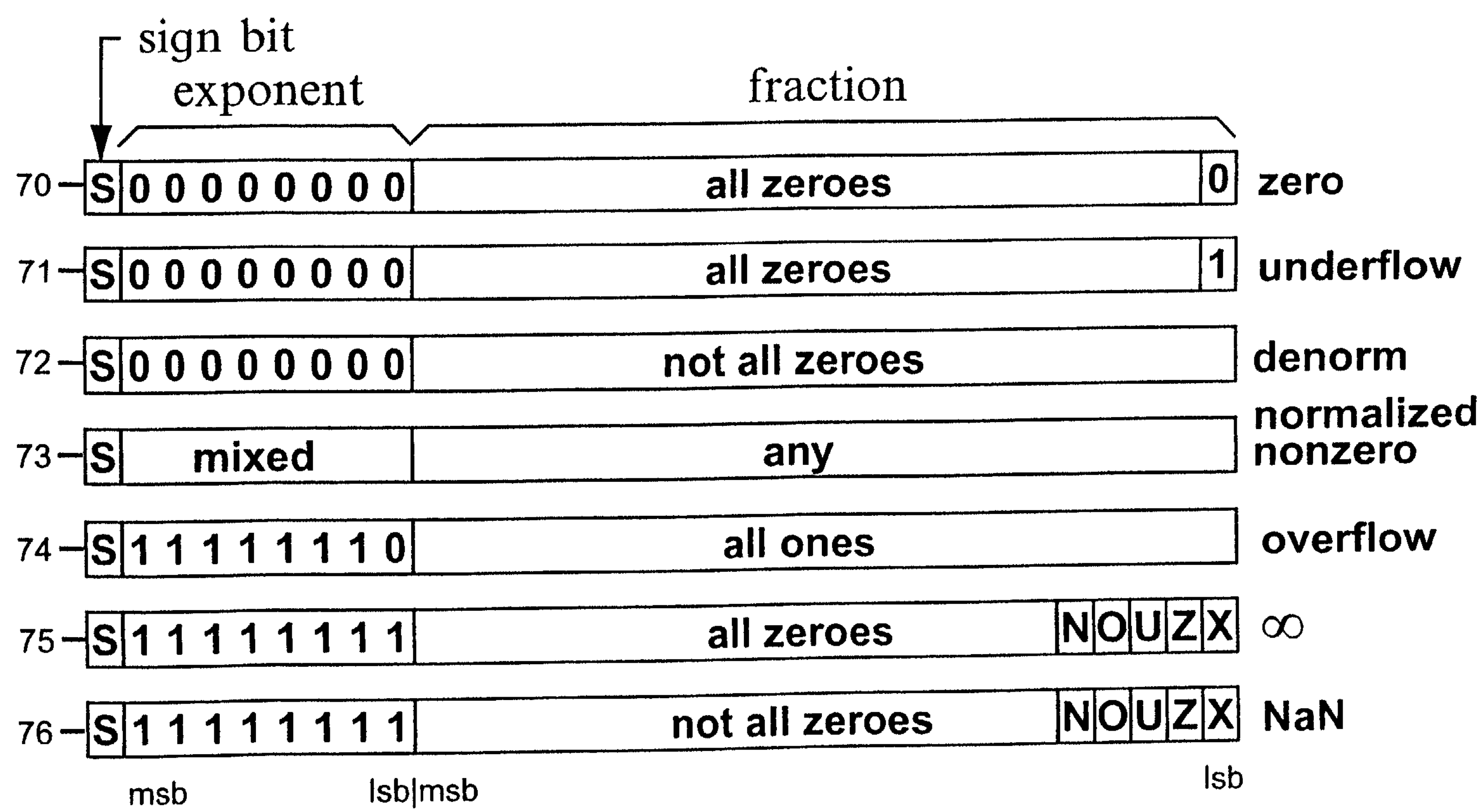


first operand 11A
second operand 11B
S
exponent
fraction (high part)
flags
32
8
18
5
20A
21A
22A
=11111111
=11111110
=00000000
30A
31A
=111111111111111111
=000000000000000000
32A
33A
34A
35A
=11111
=0000x
=00001
=00000
40A
45A
46A
47A
48A
50A
51A
52A
53
12A
12B
20B
21B
22B
30B
31B
32B
33B
34B
36B
40B
45B
46B
47B
48B
50B
51B
52B
IEEE 754 compliant
remainder core 13
result
inputs
outputs
remainder
decision
table
logic 15
mux
60
selector 61
selector 62
00000000
11111111
000000000000000000
111111111111111111
100000000000001
1
17
14
63
64
65
66
67
result

F I G. 1



sign bit
exponent
fraction
70
S 0 0 0 0 0 0 0 0
all zeroes
0
zero
71
S 0 0 0 0 0 0 0 0
all zeroes
1
underflow
72
S 0 0 0 0 0 0 0 0
not all zeroes
denorm
73
S
mixed
any
normalized nonzero
74
S 1 1 1 1 1 1 1 0
all ones
overflow
75
S 1 1 1 1 1 1 1 1
all zeroes
N O U Z X
∞
76
S 1 1 1 1 1 1 1 1
not all zeroes
N O U Z X
NaN
msb
lsb|msb
lsb

FIG. 2

rem	-oo	-OV	-Q	-UN	-0	+0	+UN	+Q	+OV	+oo	NaN
-oo	(a)	(b)	(c)	(d)	(e)	(e)	(d)	(c)	(b)	(a)	(f)
-OV	(g)	(h)	(i)	(j)	(k)	(k)	(j)	(i)	(h)	(g)	(l)
-P	-P	(m)	(n)	(o)	(p)	(p)	(o)	(n)	(m)	-P	(q)
-UN	-UN	(r)	-UN	(o)	(s)	(s)	(o)	-UN	(r)	-UN	(t)
-0	-0	(m)	-0	(o)	(p)	(p)	(o)	-0	(m)	-0	(q)
+0	+0	(m)	+0	(o)	(p)	(p)	(o)	+0	(m)	+0	(q)
+UN	+UN	(r)	+UN	(o)	(s)	(s)	(o)	+UN	(r)	+UN	(t)
+P	+P	(m)	(n)	(o)	(p)	(p)	(o)	(n)	(m)	+P	(q)
+OV	(g)	(h)	(h)	(i)	(j)	(j)	(i)	(h)	(h)	(g)	(l)
+oo	(a)	(b)	(c)	(d)	(e)	(e)	(d)	(c)	(b)	(a)	(f)
NaN	(u)	(v)	(w)	(x)	(w)	(w)	(x)	(w)	(v)	(u)	(y)

FIG. 3

```
--10----  [NaN]   --10----  [NaN]   1   *   0 001 10000 0000 11 00000  [sign(op1) NaN op1 f1|f2]
--10----  [NaN]   --10----  [NaN]   0   *   0 001 01000 0000 11 00000  [sign(op1) NaN op2 f1|f2]
--10----  [NaN]   --11----  [Inf]   -   *   0 001 10000 0000 11 00000  [sign(op1) NaN op1 f1|f2]
--10----  [NaN]   -1----1-  [OV_]   -   *   0 001 10000 0000 10 01001  [sign(op1) NaN op1 f1|ox]
--10----  [NaN]   -------1  [Q__]   -   *   0 001 10000 0000 10 00000  [sign(op1) NaN op1 f1]
--10----  [NaN]   1----1--  [UN_]   -   *   0 001 10000 0000 10 00101  [sign(op1) NaN op1 f1|ux]
--10----  [NaN]   1---1---  [0__]   -   *   0 001 10000 0000 10 00000  [sign(op1) NaN op1 f1]

--11----  [Inf]   --10----  [NaN]   -   *   0 001 01000 0000 11 00000  [sign(op1) NaN op2 f1|f2]
--11----  [Inf]   --11----  [Inf]   -   *   0 001 00001 0100 11 10000  [sign(op1) "Inf rem" f1|f2|n]
--11----  [Inf]   -1----1-  [OV_]   -   *   0 001 00001 0111 10 11001  [sign(op1) "Inf rem OV" f1|nox]
--11----  [Inf]   -------1  [Q__]   -   *   0 001 00001 0100 10 10000  [sign(op1) "Inf rem" f1|n]
--11----  [Inf]   1----1--  [UN_]   -   *   0 001 00001 0110 10 10101  [sign(op1) "Inf rem UN" f1|nux]
--11----  [Inf]   1---1---  [0__]   -   *   0 001 00001 0101 10 10000  [sign(op1) "Inf rem 0" f1|n]

-1----1-  [OV_]   --10----  [NaN]   -   *   0 001 01000 0000 01 01001  [sign(op1) NaN op2 f2|ox]
-1----1-  [OV_]   --11----  [Inf]   -   *   0 100 10000 0000 10 00000  [sign(op1) expt(op1) op1 f1]
-1----1-  [OV_]   -1----1-  [OV_]   -   *   0 001 00001 1011 00 11001  [sign(op1) "OV rem OV" nox]
-1----1-  [OV_]   -------1  [Q__]   -   *   0 001 00001 1000 00 11001  [sign(op1) "OV rem" nox]
-1----1-  [OV_]   1----1--  [UN_]   -   *   0 001 00001 1010 00 11101  [sign(op1) "OV rem UN" noux]
-1----1-  [OV_]   1---1---  [0__]   -   *   0 001 00001 1001 00 11001  [sign(op1) "OV rem 0" nox]

-------1  [P__]   --10----  [NaN]   -   *   0 001 01000 0000 01 00000  [sign(op1) NaN op2 f2]
-------1  [P__]   --11----  [Inf]   -   *   0 100 10000 0000 10 00000  [sign(op1) expt(op1) op1 f1]
-------1  [P__]   -1----1-  [OV_]   -   *   0 001 00001 0011 00 11001  [sign(op1) "rem OV" nox]
-------1  [P__]   -------1  [Q__]   -   *   1 000 00000 0000 00 00000  [IEEE 754 remainder]
-------1  [P__]   1----1--  [UN_]   -   *   0 001 00001 0010 00 10101  [sign(op1) "rem UN" nux]
-------1  [P__]   1---1---  [0__]   -   *   0 001 00001 0001 00 10000  [sign(op1) "rem 0" n]

1----1--  [UN_]   --10----  [NaN]   -   *   0 001 01000 0000 01 00101  [sign(op1) NaN op2 f2|ux]
1----1--  [UN_]   --11----  [Inf]   -   *   0 010 00100 0000 00 00001  [sign(op1) UN]
1----1--  [UN_]   -1----1-  [OV_]   -   *   0 001 00001 0011 00 11101  [sign(op1) "rem OV" noux]
1----1--  [UN_]   -------1  [Q__]   -   *   0 010 00010 0000 00 00001  [sign(op1) UN]
1----1--  [UN_]   1----1--  [UN_]   -   *   0 001 00001 0010 00 10101  [sign(op1) "rem UN" nux]
1----1--  [UN_]   1---1---  [0__]   -   *   0 001 00001 0001 00 10101  [sign(op1) "rem 0" nux]

1---1---  [0__]   --10----  [NaN]   -   *   0 001 01000 0000 01 00000  [sign(op1) NaN op2 f2]
1---1---  [0__]   --11----  [Inf]   -   *   0 010 00100 0000 00 00000  [sign(op1) 0]
1---1---  [0__]   -1----1-  [OV_]   -   *   0 001 00001 0011 00 11001  [sign(op1) "rem OV" nox]
1---1---  [0__]   -------1  [Q__]   -   *   0 010 00010 0000 00 00000  [sign(op1) 0]
1---1---  [0__]   1----1--  [UN_]   -   *   0 001 00001 0010 00 10101  [sign(op1) "rem UN" nux]
1---1---  [0__]   1---1---  [0__]   -   *   0 001 00001 0001 00 10000  [sign(op1) "rem 0" n]
```

FIG. 4